WHAT IS CLAIMED IS:

1. A level shift circuit comprising:

a capacitor;

a charge control circuit connected to the capacitor for providing a voltage of a high potential power supply to the capacitor and controlling charging of the capacitor; and

a limiting circuit connected to the high potential power supply and the charge control circuit for limiting the voltage provided to the capacitor from the high potential power supply before the charge control circuit stops providing the voltage of the high potential power supply to the capacitor.

2. A level shift circuit for converting a voltage level of an input signal to a predetermined voltage level and generating a level-shifted signal, the level shift circuit comprising:

a capacitor having a first electrode connected to a high potential power supply and a second electrode for receiving the input signal;

a charge control circuit connected to the first electrode of the capacitor for providing the voltage of the high potential power supply to the capacitor and controlling charging of the capacitor;

a first inverter for receiving the voltage of the high potential power supply and generating the level-shifted signal, wherein the first inverter includes a high potential power supply terminal connected to the first electrode of the capacitor and a low potential power supply terminal connected to the second electrode of the capacitor; and

a current limiting circuit connected to the charge control circuit for limiting the discharge current of the

capacitor.

3. The level shift circuit according to claim 2, wherein the current limiting circuit is controlled at a time different from that of the charge control circuit.

4. The level shift circuit according to claim 3, wherein the charge control circuit includes a first PMOS transistor, the gate of which receives the level-shifted signal of the first inverter.

5. The level shift circuit according to claim 4, wherein the current limiting circuit includes a second PMOS transistor, the gate of which receives the input signal.

6. The level shift circuit according to claim 5, wherein the input signal has the voltage of the high potential power supply.

7. The level shift circuit according to claim 4, further comprising:

a second inverter for generating an inverted input signal by inverting the input signal and providing the inverted input signal to the second electrode of the capacitor, wherein the second inverter includes a high potential power supply terminal for receiving the voltage of the high potential power supply and a low potential power supply terminal for receiving a voltage lower than the voltage of the high potential power supply, and wherein the current limiting circuit includes a second PMOS transistor, the gate of which receives the inverted input signal.

8. The level shift circuit according to claim 7,

wherein the input signal has the voltage of the high potential power supply.

9. The level shift circuit according to claim 4, further comprising:

a second inverter for generating an inverted input signal by inverting the input signal and providing the inverted input signal to the second electrode of the capacitor, wherein the second inverter includes a high potential power supply terminal for receiving the voltage of the high potential power supply and a low potential power supply terminal for receiving a voltage lower than the voltage of the high potential power supply, wherein the current limiting circuit includes a second PMOS transistor and a third inverter connected to a gate of the second PMOS transistor, wherein the third inverter includes a high potential power supply terminal for receiving the voltage of the high potential power supply and a low potential power supply terminal for receiving a voltage lower than the voltage of the high potential power supply, and wherein the third inverter generates an inverted input signal by inverting the input signal and provides the inverted input signal to the gate of the second PMOS transistor.

10. The level shift circuit according to claim 9, wherein the input signal has the voltage of the high potential power supply.

11. A level shift circuit comprising:

a shift circuit for receiving an input signal and level-shifting the voltage of the input signal to generate a level-shifted signal, the shift circuit including;

first and second transistors having the same

polarity, wherein the sources of the first and second transistors are connected to a first power supply having a first voltage, the gate of the first transistor being connected to the drain of the second transistor, and the gate of the second transistor being connected to the drain of the first transistor;

third and fourth transistors having a polarity opposite of the polarity of the first or second transistor, wherein the sources of the third and fourth transistors are connected to a second voltage source having a second voltage that is lower than the first voltage;

a fifth transistor connected between the first transistor and the third transistor and having the same polarity as the third transistor; and

a sixth transistor connected between the second transistor and the fourth transistor and having the same polarity as the fourth transistor; and

a voltage generation circuit connected to the shift circuit for generating a gate control voltage, which is provided to the gates of the fifth transistor and the sixth transistor based on the first voltage.

12. The level shift circuit according to claim 11, wherein the withstand voltages of the third and fourth transistors are lower than the withstand voltages of the first, second, fifth, and sixth transistors.

13. The level shift circuit according to claim 12, wherein the voltage generation circuit includes:

a plurality of transistors connected between the first and second power supplies for dividing the differential voltage between the first voltage and the

second voltage so to generate the gate control voltage, wherein the plurality of transistors are connected in series and have the same polarity.

14. The level shift circuit according to claim 13, further comprising:

an input circuit connected to the second power supply and a third power supply for receiving and providing the input signal to the gate of the fourth transistor, and for receiving the input signal and inverting the input signal to provide an inverted input signal to the gate of the third transistor, wherein the third power supply has a third voltage that is lower than the first voltage and higher than the second voltage.

15. The level shift circuit according to claim 14, wherein the voltage generation circuit generates the gate control voltage based on a control signal.

16. The level shift circuit according to claim 15, further comprising:

a protection circuit connected between the shift circuit and the voltage generation circuit to prevent the gate control voltage from being provided to the gates of the fifth and sixth transistors, until the gate control voltage reaches a predetermined voltage.

17. The level shift circuit according to claim 16, wherein the protection circuit connects the gates of the fifth and sixth transistors to the second power supply until the gate control voltage reaches the predetermined voltage.

18. The level shift circuit according to claim 17,

wherein the protection circuit includes:

a first switch circuit connected to the shift circuit and the voltage generation circuit, wherein the first switch circuit is deactivated when the gate control voltage is higher than the predetermined voltage; and

a second switch circuit connected to the shift circuit and the second power supply, wherein the second switch circuit and the first switch circuit are activated and deactivated in a complementary manner, and wherein the second switch circuit is activated when the first switch circuit is deactivated, so to connect the gates of the fifth and sixth transistors to the second power supply.

19. The level shift circuit according to claim 18, wherein the voltage generation circuit generates a first control voltage that differs from the gate control voltage, and wherein the protection circuit further includes:

a switch signal generation circuit connected to the voltage generation circuit for generating a switch signal, which activates and deactivates the first switch circuit based on a first control voltage.

20. The level shift circuit according to claim 12, wherein the voltage generation circuit includes:

a plurality of transistors connected between the first power supply and a third power supply having a third voltage lower than the first voltage and higher than the second voltage, wherein the plurality of transistors divide the differential voltage between the first voltage and the third voltage so to generate the gate control voltage, and wherein the plurality of

transistors are connected in series and have the same polarity.

21. The level shift circuit according to claim 20, further comprising:

an input circuit connected between the second power supply and the third power supply for receiving and providing the input signal to the gate of the fourth transistor and for receiving the input signal and inverting the input signal to provide an inverted input signal to the gate of the third transistor.

22. The level shift circuit according to claim 21, wherein the voltage generation circuit generates the gate control voltage based on a predetermined control signal.

23. The level shift circuit according to claim 22, further comprising:

a protection circuit connected between the shift circuit and the voltage generation circuit so to prevent the gate control voltage from being provided to the gates of the fifth and sixth transistors, until the gate control voltage reaches a predetermined voltage.

24. The level shift circuit according to claim 23, wherein the protection circuit connects the gates of the fifth and sixth transistors to the second power supply until the gate control voltage reaches the predetermined voltage.

25. The level shift circuit according to claim 11, wherein the voltage generation circuit includes:

a plurality of transistors connected between the first power supply and the second power supply for

dividing the differential voltage between the first voltage and the second voltage to generate the gate control voltage, wherein the plurality of transistors are connected in series and have the same polarity.

26. The level shift circuit according to claim 25, further comprising:

a protection circuit connected between the shift circuit and the voltage generation circuit to prevent the gate control voltage from being provided to the gates of the fifth and sixth transistors, until the gate control voltage reaches a predetermined voltage.

27. The level shift circuit according to claim 11, wherein the voltage generation circuit includes:

a plurality of transistors connected between the first power supply and a third power supply having a third voltage lower than the first voltage and higher than the second voltage, wherein the plurality of transistors divide the differential voltage between the first voltage and the third voltage so to generate the gate control voltage, wherein the plurality of transistors are connected in series and have the same polarity.

28. The level shift circuit according to claim 27, further comprising:

a protection circuit connected between the shift circuit and the voltage generation circuit to prevent the gate control voltage from being provided to the gates of the fifth and sixth transistors, until the gate control voltage reaches a predetermined voltage.

29. The level shift circuit according to claim 11, wherein the voltage generation circuit generates the gate control voltage so that the source-drain voltage of the third transistor is lower than the withstand voltage of the third transistor and the source-drain voltage of the fourth transistor is lower than the withstand voltage of the fourth transistor.

30. A semiconductor device including a level shift circuit, the level shift circuit comprising:

a shift circuit for receiving an input signal and level-shifting the voltage of the input signal to generate a level-shifted signal, the shift circuit including;

first and second transistors having the same polarity, wherein the sources of the first and second transistors are connected to a first power supply having a first voltage, the gate of the first transistor is connected to the drain of the second transistor, and the gate of the second transistor is connected to the drain of the first transistor;

third and fourth transistors having a polarity opposite of the polarity of the first or second transistor, wherein the sources of the third and fourth transistors are connected to a second voltage source having a second voltage that is lower than the first voltage;

a fifth transistor connected between the first transistor and the third transistor and having the same polarity as the third transistor; and

a sixth transistor connected between the second transistor and the fourth transistor and having the same polarity as the fourth transistor; and

a voltage generation circuit connected to the shift

circuit for generating a gate control voltage, which is provided to the gates of the fifth transistor and the sixth transistor based on the first voltage.

31. The semiconductor device according to claim 30, wherein the voltage generation circuit includes:

a plurality of transistors connected between the first and second power supplies for dividing the differential voltage between the first voltage and the second voltage so to generate the gate control voltage, wherein the plurality of transistors are connected in series and have the same polarity.

32. The semiconductor device according to claim 31, the level shift circuit further comprising:

a protection circuit connected between the shift circuit and the voltage generation circuit to prevent the gate control voltage from being provided to the gates of the fifth and sixth transistors, until the gate control voltage reaches a predetermined voltage.

33. The semiconductor device according to claim 30, wherein the voltage generation circuit includes:

a plurality of transistors connected between the first power supply and a third power supply having a third voltage lower than the first voltage and higher than the second voltage, wherein the plurality of transistors divide the differential voltage between the first voltage and the third voltage so to generate the gate control voltage, and wherein the plurality of transistors are connected in series and have the same polarity.

34. The semiconductor device according to claim 33, the level shift circuit further comprising:

a protection circuit connected between the shift circuit and the voltage generation circuit to prevent the gate control voltage from being provided to the gates of the fifth and sixth transistors, until the gate control voltage reaches a predetermined voltage.

35. The semiconductor device according to claim 30, wherein the voltage generation circuit generates the gate control voltage so that the source-drain voltage of the third transistor is lower than the withstand voltage of the third transistor and the source-drain voltage of the fourth transistor is lower than the withstand voltage of the fourth transistor.